SONY

CXP854P60

CMOS 8-bit Single-chip Microcomputer

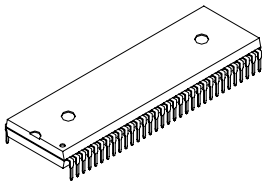
Description

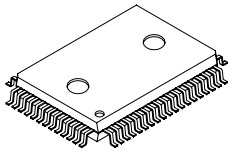
The CXP854P60 are a highly integrated microcomputers composed of a 8-bit CPU, PROM, RAM, and I/O ports. These chips feature many other high-performance circuits in a single-chip CMOS design, including an A/D converter, serial interface, timer/counter, time-base timer, vector interrupt, on-screen display function, I²C bus interface, PWM generator, remote control receiver, HSYNC counter, and watchdog timer.

Also, the CXP854P60 provides power-on reset and sleep functions. The designers have ensured low power consumption for these powerful microcomputers.

Incorporating a one-time PROM, the CXP854P60 has an equivalent function to the CXP85460 and character ROM for OSD can be written. Therefore, it is suitable for evaluation in system development and for the production of small amounts.

64 pin SDIP (PIastic) 64 pin QFP (PIastic)





Structure

Silicon gate CMOS IC

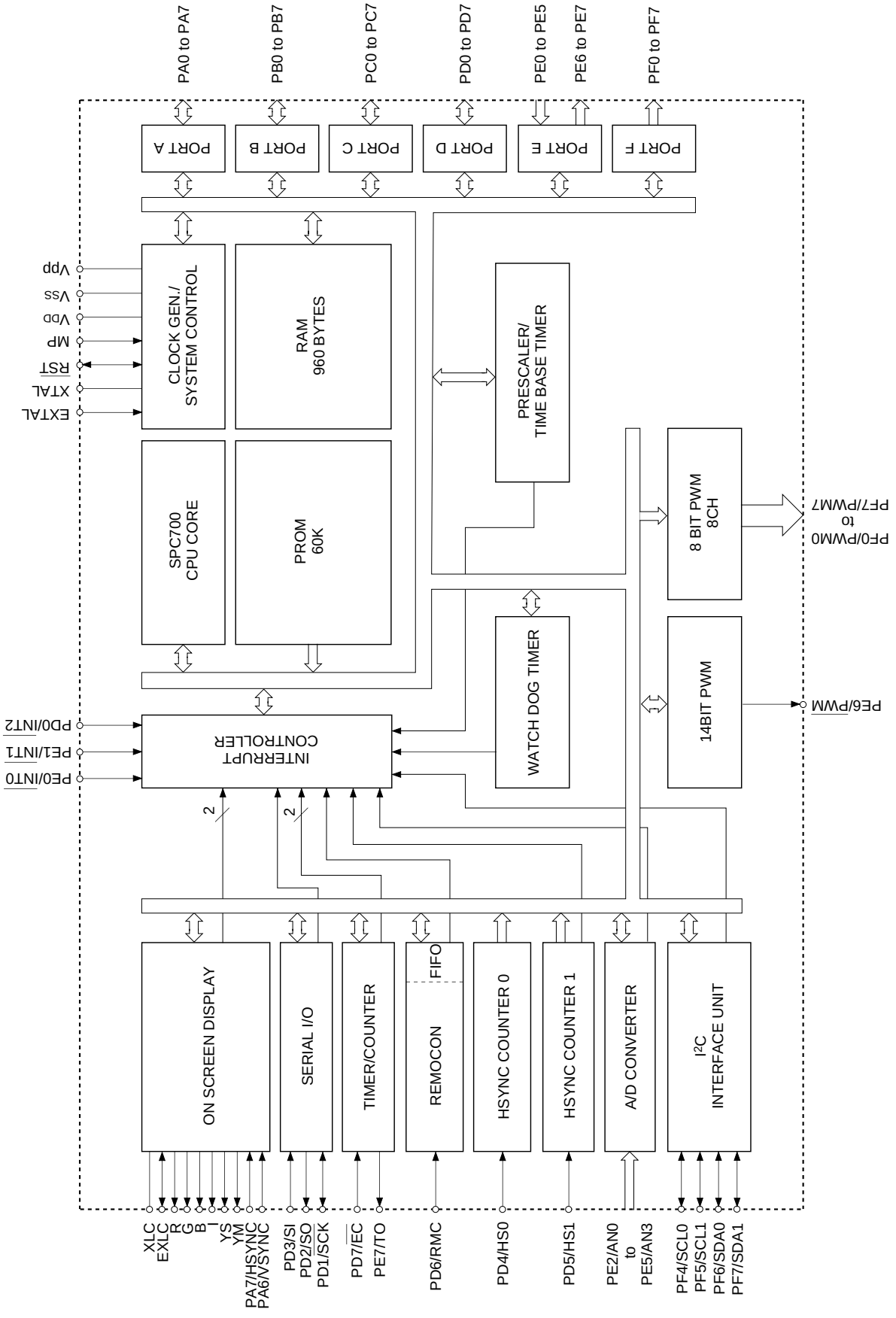
Features

- Instruction set which supports a wide array of data types-213 types of instructions which include 16-bit calculations, multiplication and division arithmetic, and boolean operations.
- Minimum instruction cycle 0.5µs/8MHz
- On-chip PROM 60K bytes (For program)
  10K bytes (For OSD)
- On-chip RAM 960 bytes
- On-screen display function 12 × 18 dots, 384 types, 12lines of 32 characters
  Black frame output, half blanking, shadow, background color on full screen
  Double scanning mode supported includes jitter elimination circuit
- I²C bus interface
- 14-bit PWM output, 8-bit PWM output (8 channels)
- Remote control receiver circuit
- 8-bit A/D converter (4 channels, 20µs conversion time/4MHz, 8MHz)
- HSYNC counter (2channels)
- Watchdog timer
- 8-bit synchronized serial I/O
- 8-bit timer, 8-bit timer/counter, 19-bit time-base timer
- General purpose input/output 32-line I/O (bit-selectable input/output), also 6-line input, 10-line output (internal 8-line Nch-O/D)
- Interrupts 13 factors, 13 vectors, multiple interrupt possible
- Standby mode SLEEP
- Package 64-pin plastic SDIP/QFP

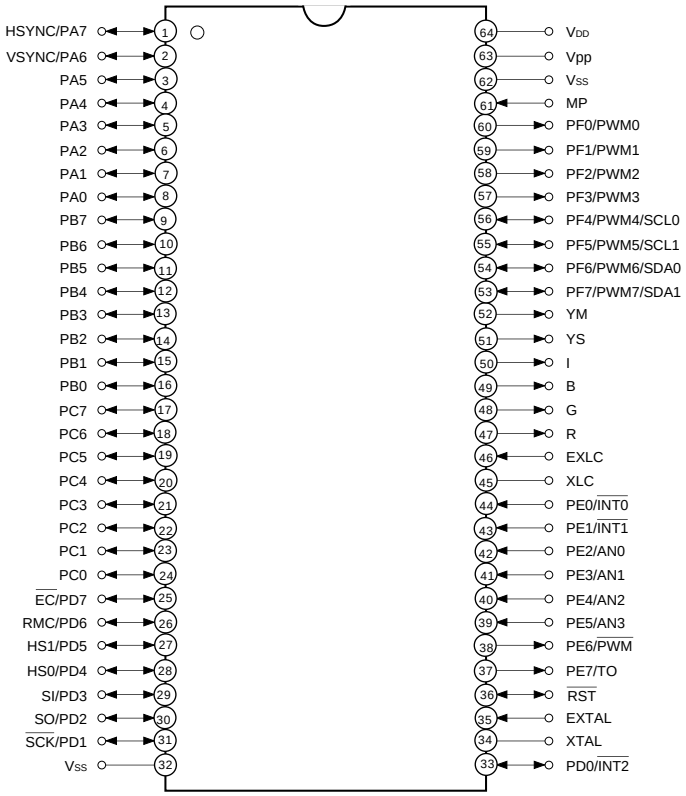
Purchase of Sony's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specifications as defined by Philips.

E95109A16-PS

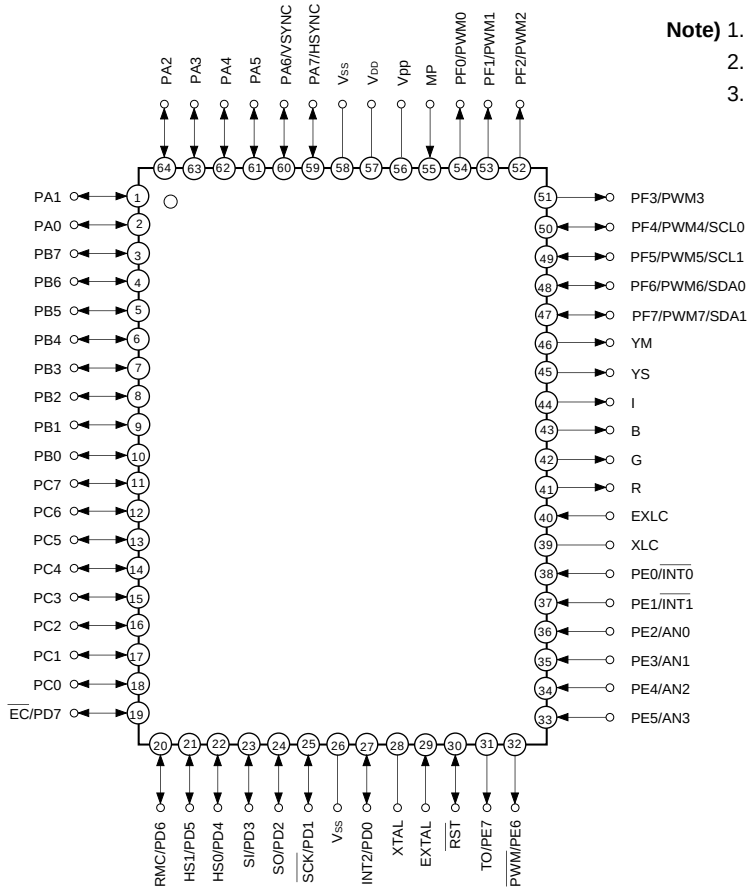
Block Diagram



Pin Assignment (Top View)



Note) 1. Vpp pin 63 must be connected to V_{DD}.
2. Vss pins 32 and 62 must have a common GND.
3. MP pin 61 must be connected to GND.



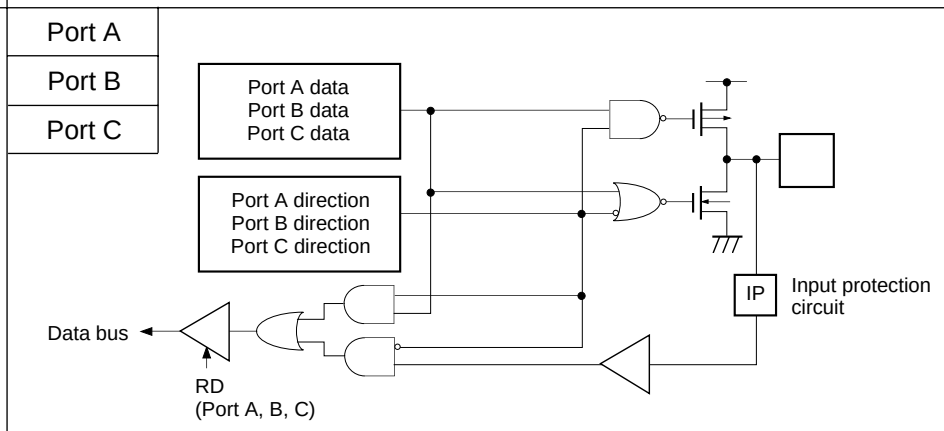
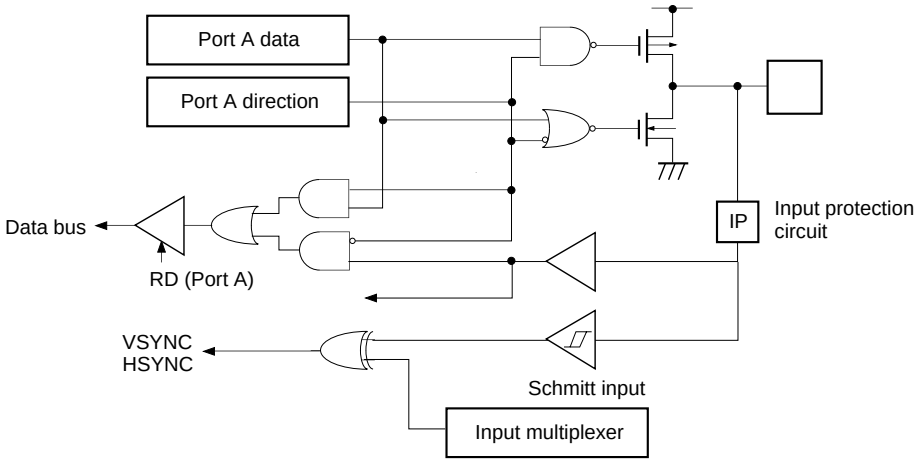
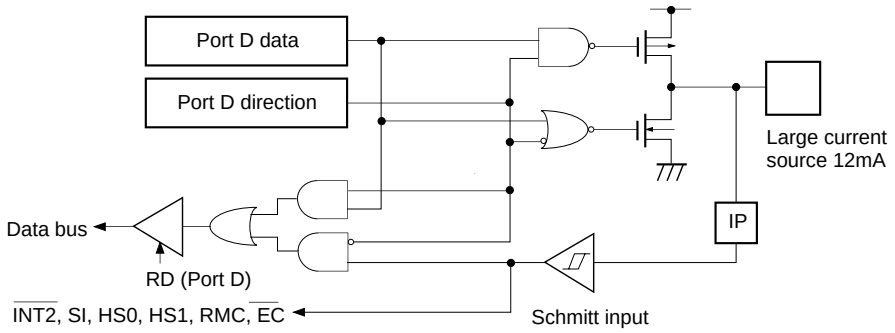
Note) 1. Vpp pin 56 must be connected to V_{DD}.
2. Vss pins 26 and 58 must have a common GND.
3. MP pin 55 must be connected to GND.

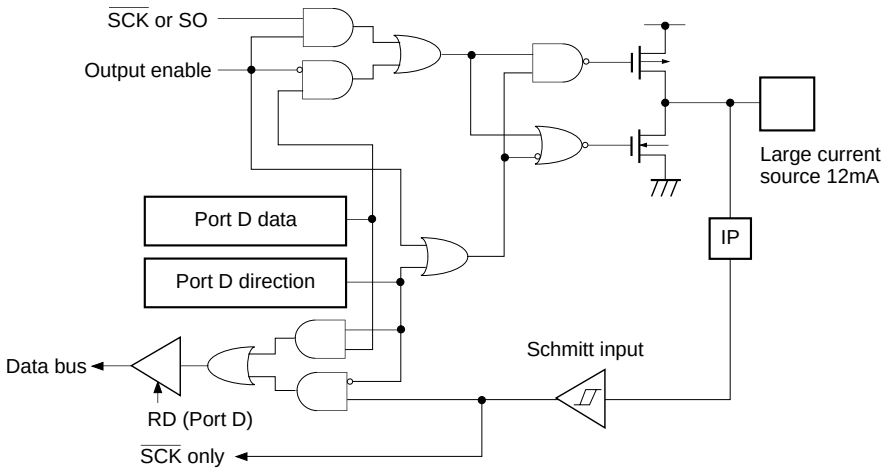
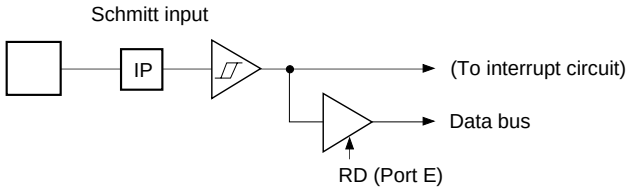
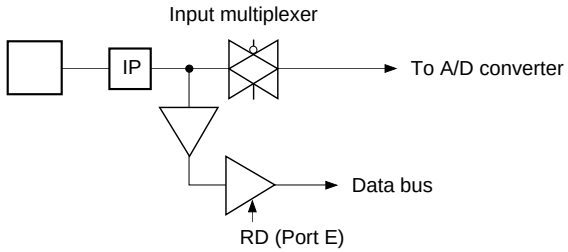
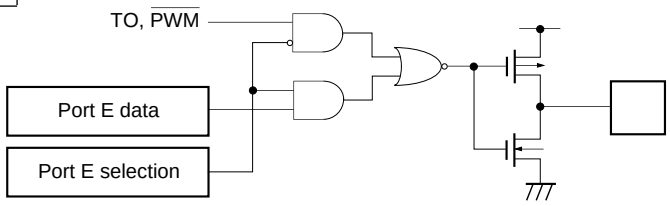
Pin Functions

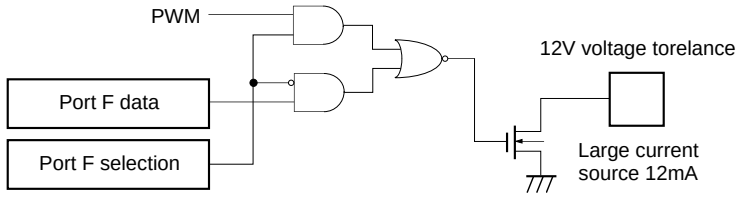
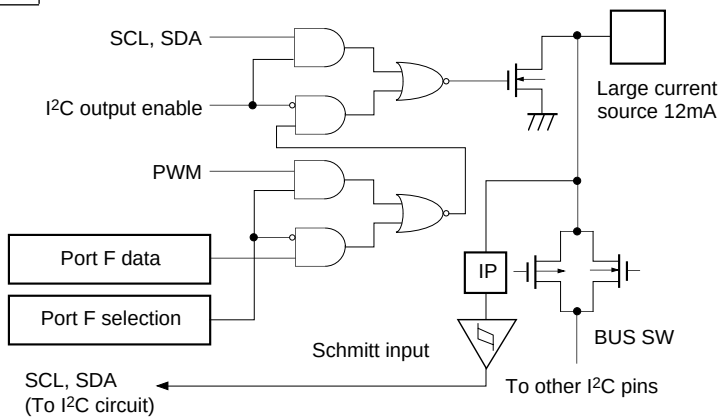
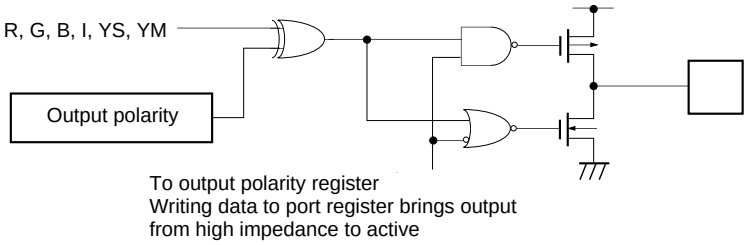
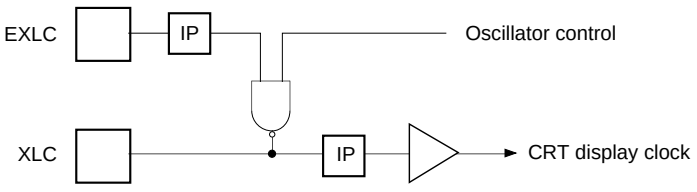
Pin Name	I/O	Function	
PA0 to PA5	I/O	(Port A) Single bit selectable 8-bit port. (8 lines)	
PA6/VSYNC	I/O/Input		CRT display vertical synchronization signal input pin.
PA7/HSYNC	I/O/Input		CRT display horizontal synchronization signal input pin.
PB0 to PB7	I/O	(Port B) Single bit selectable 8-bit port. (8 lines)	
PC0 to PC7	I/O	(Port C) Single bit selectable 8-bit port. (8 lines)	
PD0/$\overline{\text{INT2}}$	I/O/Input	(Port D) Single bit selectable 8-bit port. 12mA sink current drive possible. (8 lines)	Input pin for external interrupt request. Active on falling edge.
PD1/$\overline{\text{SCK}}$	I/O/I/O		Serial clock pin.
PD2/SO	I/O/Output		Serial data output pin.
PD3/SI	I/O/Input		Serial data input pin.
PD4/HS0	I/O/Input		HSYNC counter (CH0) input pin.
PD5/HS1	I/O/Input		HSYNC counter (CH1) input pin.
PD6/RMC	I/O/Input		Remote control receiver circuit input pin.
PD7/$\overline{\text{EC}}$	I/O/Input		External event timer/counter input pin.
PE0/$\overline{\text{INT0}}$ PE1/$\overline{\text{INT1}}$	Input/Input	(Port E) 8-bit port, lower 6 bits for input, upper 2 bits for output. (8 lines)	Input pin for external interrupt request. Active falling edge. (2 lines)
PE2/AN0 to PE5/AN3	Input/Input		Analog input pin for A/D converter. (4 lines)
PE6/$\overline{\text{PWM}}$	Output/Output		14-bit PWM output pin. (CMOS output)
PE7/TO	Output/Output		Square wave output for timer 1. (50% duty cycle)
PF0/PWM0 to PF3/PWM3	Output/Output	(Port F) 8-bit output port with large current (12mA) N-ch open drain output. Lower 4 bits middle voltage tolerance (12V), upper 4 bits 5V suppression. (8 lines)	8-bit PWM output pin. (8-lines)
PF4/PWM4/ SCL0 PF5/PWM5/ SCL1	Output/Output/ I/O		I^2C bus interface transfer clock I/O pin.
PF6/PWM6/ SDA0 PF7/PWM7/ SDA1	Output/Output/ I/O		I^2C bus interface transfer data I/O pin.
R, G, B, I, YS, YM	Output	CRT display 6-bit output pin.	

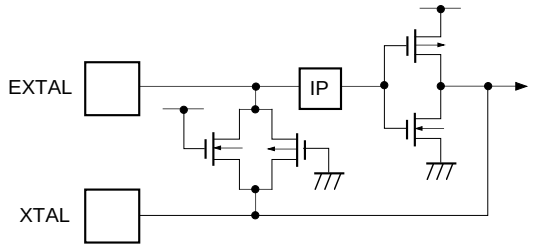
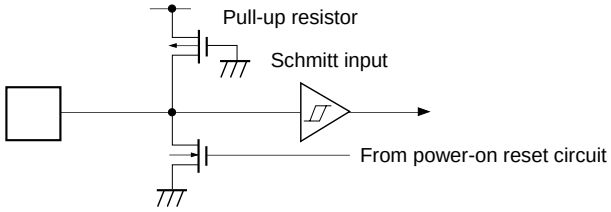
Pin Name	I/O	Function
EXLC	Input	CRT display clock oscillator I/O pin. Oscillator frequency is determined external L, C circuit.
XLC	Output	
EXTAL	Input	System clock oscillator crystal connection pin. When using an external clock, input to EXTAL pin and leave XTAL pin open.
XTAL	Output	
$\overline{RST}$	I/O	"L" level active system reset. This pin also acts as an I/O pin during power up. While internal power-on reset function is talking place a "L" level is output.
MP	Input	Test mode input pin. Must be connected to GND.
Vpp		Positive power supply pin for incorporated PROM writing. Under normal operating conditions, connect to V_{DD}.
V_{DD}		Positive supply voltage pin.
Vss		GND. Both Vss pins should be connected to common GND.

Pin Equivalent I/O Circuit

Pin	Circuit format	When reset
PA0 to PA5 PB0 to PB7 PC0 to PC7 22 lines	Port A Port B Port C 	Hi-Z
PA6/VSYNC PA7/HSYNC 2 lines	Port A 	Hi-Z
PD0/$\overline{\text{INT2}}$ PD3/SI PD4/HS0 PD5/HS1 PD6/RMC PD7/$\overline{\text{EC}}$ 6 lines	Port D 	Hi-Z

Pin	Circuit format	When reset
PD1/$\overline{SCK}$ PD2/SO 2 lines	Port D 	Hi-Z
PE0/$\overline{INT0}$ PE1/$\overline{INT1}$ 2 lines	Port E 	Hi-Z
PE2/AN0 to PE5/AN3 4 lines	Port E 	Hi-Z
PE6/$\overline{PWM}$ PE7/TO 2 lines	Port E 	H level

Pin	Circuit format	When reset
PF0/PWM0 to PF3/PWM3 4 lines	Port F 	Hi-Z
PF4/PWM4/ SCL0 PF5/PWM5/ SCL1 PF6/PWM6/ SDA0 PF7/PWM7/ SDA1 4 lines	Port F 	Hi-Z
R G B I YS YM 6 lines		Hi-Z
EXLC XLC 2 lines		Oscillation halted

Pin	Circuit format	When reset
EXTAL XTAL 2 lines		Oscillation
$\overline{\text{RST}}$ 1 line		L level

Absolute Maximum Ratings (Vss = 0V)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	Vpp	–0.3 to +13.0	V	Incorporated PROM
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
Medium voltage tolerance output voltage	V_{OUTP}	–0.3 to +15.0	V	Pins PF0 to PF3
High level output current	I_{OH}	–5	mA	
High level total output current	$\sum I_{OH}$	–50	mA	Total of all output pins
Low level output current	I_{OL}	15	mA	Excludes large current output
	I_{OLC}	20	mA	Large current output*2
Low level total output current	$\sum I_{OL}$	130	mA	Total of all output pins
Operating temperature	Topr	–10 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	1000	mW	SDIP
		600	mW	QFP

*1 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*2 The large current driver for the PD and PF ports is a N-ch transistor.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss =0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Safe operating range
		3.5	5.5	V	Safe operating range for low speed data*1
		2.5	5.5	V	Safe operating range for data retention during STOP
	Vpp	Vpp = V_{DD}		V	*5
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	I^2C Schmitt input included*2
	V_{IHS}	0.8V_{DD}	V_{DD}	V	CMOS Schmitt input*3
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL pin*4
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	I^2C Schmitt input included*2
	V_{ILS}	0	0.2V_{DD}	V	CMOS Schmitt input*3
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*4
Operating temperature	Topr	–10	+75	°C	

*1 Rating for 1/16 frequency mode and sleep mode.

*2 Normal input port (All pins PA, PB, PC, PE2 to PE5), PF4 to PF7 pins.

*3 Includes PD0/$\overline{INT2}$, PD1/$\overline{SCK}$, PD2, PD3/SI, PD4/HS0, PD5/HS1, PD6/RMC, PD7/$\overline{EC}$, PE0/$\overline{INT0}$, PE1/$\overline{INT1}$, HSYNC, VSYNC, $\overline{RST}$ pins.

*4 Rating applies to external clock input only.

*5 Vpp and V_{DD} should be set to a same voltage.

DC Characteristics (Ta = –10 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE6, PE7, R, G, B, I, YS, YM	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}	PA to PD, PE6, PE7, R, G, B, I, YS, YM, PF0 to PF3, $\overline{RST}$	V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PF	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	V_{DD} = 4.5V, I_{OL} = 3.0mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 4.0mA			0.6	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{IHL}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{ILR}	$\overline{RST}$	V_{DD} = 5.5V, V_{IL} = 0.4V	–1.5		–400	µA
I/O leakage current	I_{IZ}	PA to PE, HSYNC, VSYNC, R, G, B, I, YS, YM	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Open drain output leak current (N-ch Tr off case)	I_{LOH}	PF0 to PF3	V_{DD} = 5.5V, V_{OH} = 12.0V			50	µA
		PF4 to PF7	V_{DD} = 5.5V, V_{OH} = 5.5V			10	µA
I^2C bus switch connection impedance (Output Tr off case)	R_{BS}	SCL0: SCL1 SDA0: SDA1	V_{DD} = 4.5V V_{SCL0} = V_{SCL1} = 2.25V V_{SDA0} = V_{SDA1} = 2.25V			120	Ω
Supply current	I_{DD}	V_{DD}*1	Operating mode (1/2, clock rate) 8MHz crystal oscillator (C_1 = C_2 = 22pF) All output pins open		20	35	mA
	I_{DDSL}		SLEEP mode		1.0	3	mA
	I_{DDST}		STOP mode*2	—	—	—	µA
Input capacitance	C_{IN}	Pins other than V_{DD} and Vss	1MHz clock 0V for non-measurement pins		10	20	pF

*1 Rating applies only if OSD oscillator is halted.

*2 This device does not enter in the stop mode.

AC Characteristics

(1) Clock timing (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	System	Pin	Condition	Min.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	3.5	9	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	50		ns
System clock rise and fall times	t_{CR}, t_{CF}	EXTAL	Fig 1, Fig 2 External clock drive		200	ns
Event counter input clock pulse widtth	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	tsys + 50*		ns
Event counter input clock rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3		20	ms

* tsys indicates one of three values according to the contents of the clock control register. (For CPU clock selection.)
tsys (ns) = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

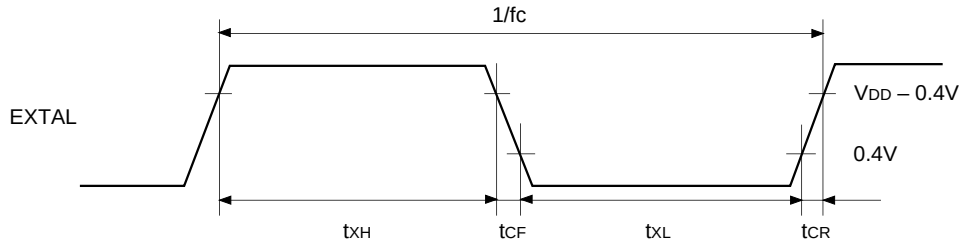


Fig. 2. Clock applied condition

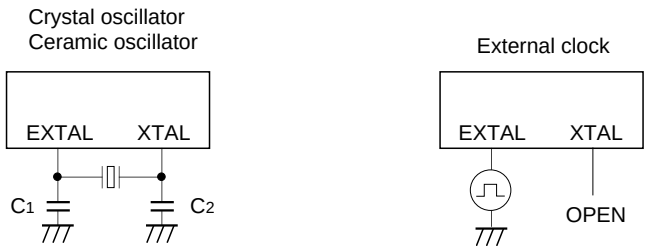
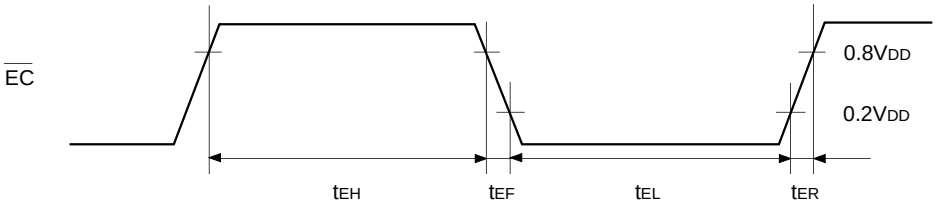


Fig. 3. Event count clock timing

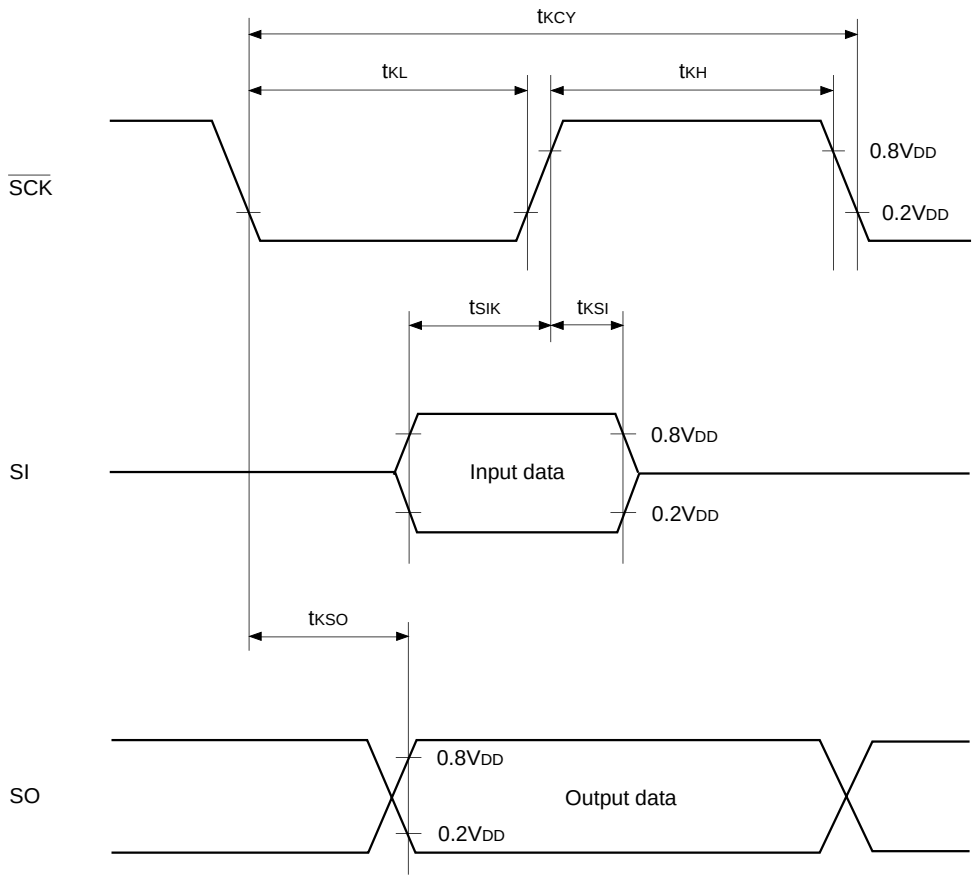


(2) Serial transfer (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	System	Pin	Condition	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK}$	$\overline{SCK}$ input mode	400		ns
			$\overline{SCK}$ output mode	4000/fc – 50		ns
SI input set-up time (referenced to $\overline{SCK}$ ↑)	t_{SIK}	SI	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (referenced to $\overline{SCK}$ ↑)	t_{KSI}	SI	$\overline{SCK}$ input mode	200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}$ ↓ → SO delay time	t_{KSO}	SO	$\overline{SCK}$ input mode		200	ns
			$\overline{SCK}$ output mode		100	ns

Note) For $\overline{SCK}$ output mode, in addition to output delay time SO capacitance must be 50pF + 1TTL.

Fig. 4. Serial transfer timing



(3) Interrupt, Reset input (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interrupt high and low level widths	t_{IH} t_{IL}	$\overline{INT0}$ to $\overline{INT2}$		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		8/fc		µs

Fig. 5. Interrupt input timing

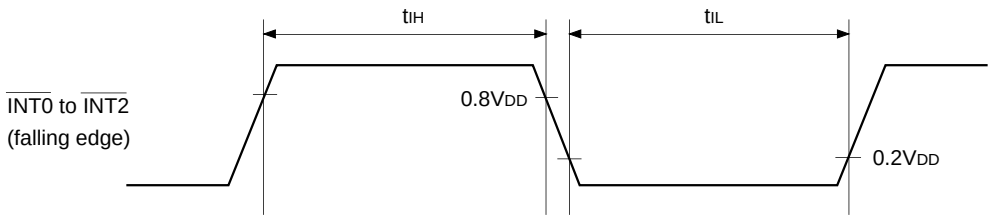
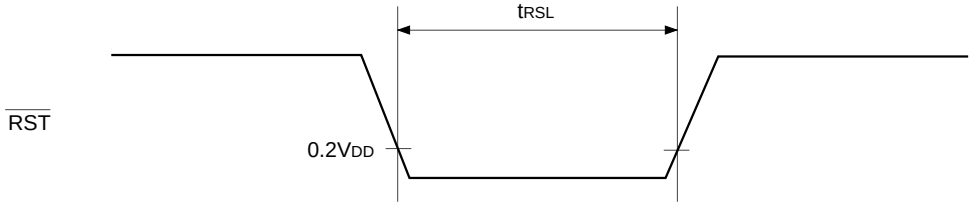


Fig. 6. $\overline{RST}$ input timing

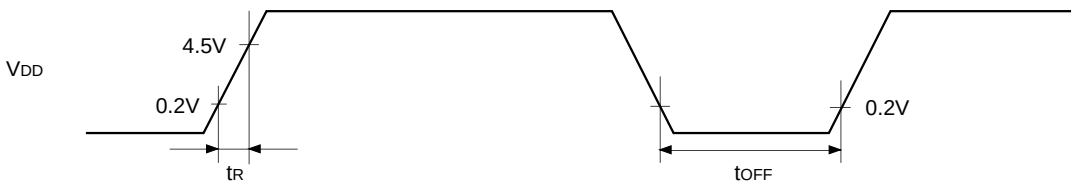


(4) Power-on reset

Power on reset (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rise time	t_R	V_{DD}	Power-on reset	0.05	50	ms
Power supply cutt-off time	t_{OFF}		Repeated power-on reset	1		ms

Fig. 7. Power-on reset

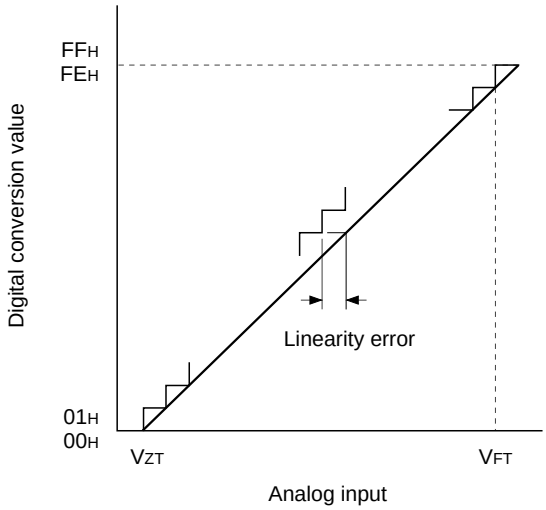


Take care when turning on power.

(5) A/D converter characteristics (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = 5.0V Vss = 0V			±1	LSB
Zero transition voltage	V_{ZT}*1			–10	10	70	mV
Full-scale transition voltage	V_{FT}*2			4910	4970	5030	mV
Conversion time	t_{CONV}			160/f_{ADC}*3			µs
Sampling time	t_{SAMP}			12/f_{ADC}*3			µs
Analog input voltage	V_{IAN}	AN0 to AN3		0		V_{DD}	V

Fig. 8. Definitions for A/D converter terms



*1 V_{ZT}: Digital conversion values change between $00_H \longleftrightarrow 01_H$.

*2 V_{FT}: Digital conversion values change between $0E_H \longleftrightarrow 0F_H$.

*3 f_{ADC} indicates the below values due to the bit6 (CKS) of A/D control registor (address: $00F6_H$) and the Bit 7 (PCK1) and Bit 6 (PCK0) of clock control registor (address: $00FE_H$)

CKS / PCK1, 0	0 (ϕ/2 selection)	1 (ϕ/2 selection)
00 (ϕ = f_{EX}/2)	f_{ADC} = f_C/2	f_{ADC} = f_C
01 (ϕ = f_{EX}/4)	f_{ADC} = f_C/4	f_{ADC} = f_C/2
11 (ϕ = f_{EX}/16)	f_{ADC} = f_C/16	f_{ADC} = f_C/8

(6) I²C bus timing (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCL clock frequency	f_{SLC}	SCL		0	100	kHz
Bus free time before starting transfer	t_{BUF}	SDA, SCL		4.7		µs
Hold time for starting transfer	$t_{HD; STA}$	SDA, SCL		4.0		µs
Clock low level width	t_{LOW}	SCL		4.7		µs
Clock high level width	t_{HIGH}	SCL		4.0		µs
Set-up time for repeated transfers	$t_{SU; STA}$	SDA, SCL		4.7		µs
Data hold time	$t_{HD; DAT}$	SDA, SCL		0*		µs
Data set-up time	$t_{SU; DAT}$	SDA, SCL		0.25		µs
SDA, SCL rise time	t_R	SDA, SCL			1	µs
SDA, SCL fall time	t_F	SDA, SCL			0.3	µs
Set-up time for transfer completion	$t_{SU; STO}$	SDA, SCL		4.7		µs

* Since SCL rise time (max: 300ns) is not considered part of data hold time, allow at least 300ns.

Fig. 9. I²C bus transfer data timing

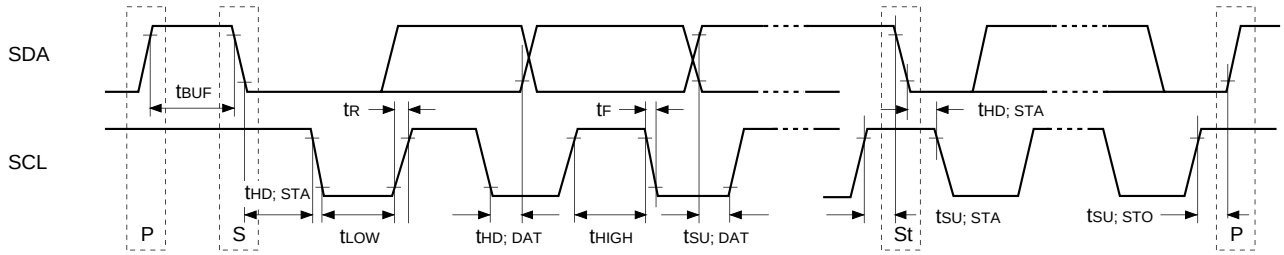
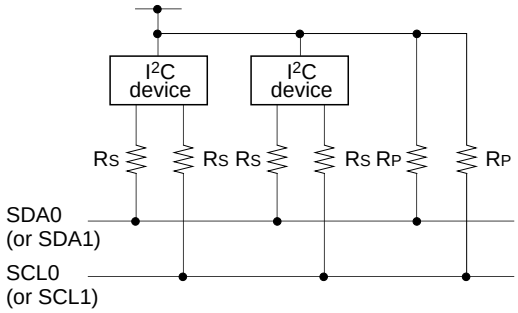


Fig. 10. I²C device suggested circuit



- A pull-up resistor must be connected to SDA0 (or SDA1), and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (Rs = 300Ω or less) can be used to reduce spike noise caused by CRT flashover.

(7) OSD (On Screen Display) timing (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condiiton	Shadow Existent		Shadow Non-existent		Unit
				Min.	Max.	Min.	Max.	
OSD clock frequency	f_{OSC}	EXLC XLC	Fig. 12	4	7*1	4	11*1	MHz
					14*2		16*2	
HSYNC pulse width	t_{HWD}	HSYNC	Fig. 11	1.2		1.2		µs
HSYNC afterwrite rise and fall times	t_{HCG}	HSYNC	Fig. 11		200		200	ns
VSYNC afterwrite rise and fall times	t_{VCG}	VSYNC	Fig. 11		1.0		1.0	µs

*1 Oscillator clock at 4MHz operation

*2 Oscillator clock at 8MHz operation

Fig. 11. OSD timing

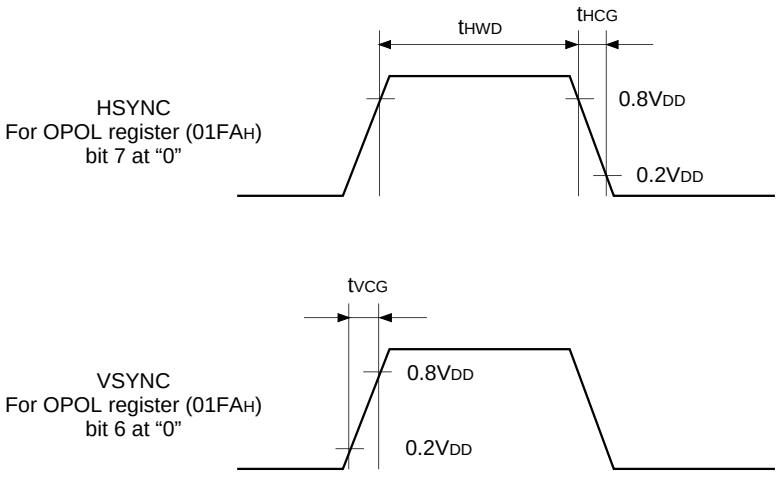
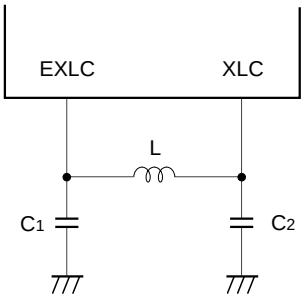
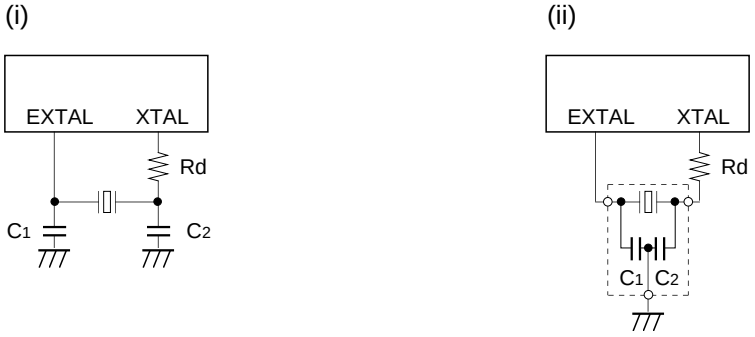


Fig. 12. LC oscillator circuit connection



Supplement

Fig. 13. SPC700 Series recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit Example
MURATA MFG CO., LTD.	CSA4.00MG	4.00	30	30	0	(i)
	CSA4.19MG	4.19				
	CSA8.00MTZ	8.00				
	CST4.00MGW*	4.00				(ii)
	CST4.19MGW*	4.19				
	CST8.00MTW*	8.00				
RIVER ELETEC CO., LTD.	HC-49/U03	4.00	12	12	0	(i)
		4.19				
		8.00				
KINSEKI LTD.	HC-49/U(-S)	4.00	27	27	0	(i)
		4.19				
		8.00				

* Indicates types with on-chip grounding capacitors (C_1 and C_2).

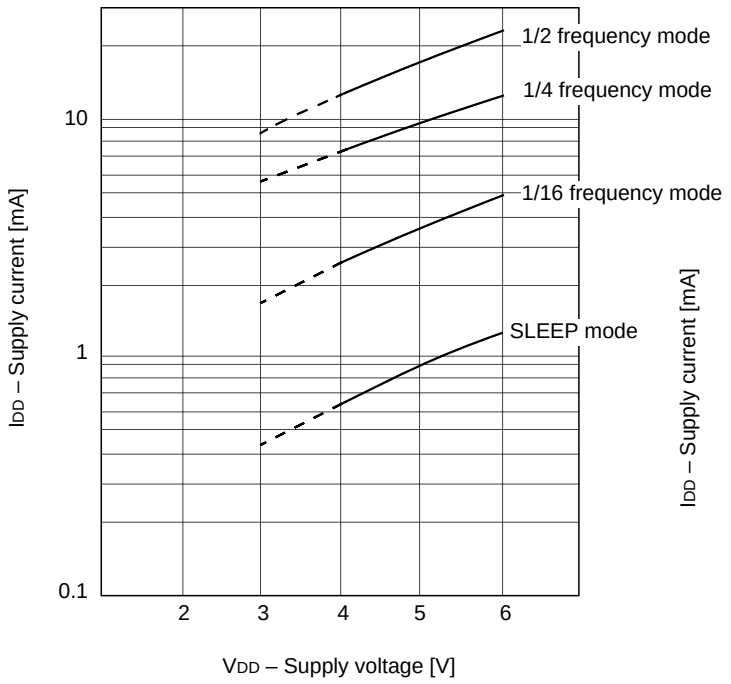
Product List

Option item	Mask product	CXP854P60S-1-☐☐☐ CXP854P60Q-1-☐☐☐
Package	64-pin plastic SDIP/QFP	64-pin plastic SDIP/QFP
Program ROM capacitance	52K/60K byte	PROM 60K byte
Reset pin pull-up resistor	Existent/Non-existent	Existent
Power-on reset circuit	Existent/Non-existent	Existent
Font data	User specified	User specified (PROM)*

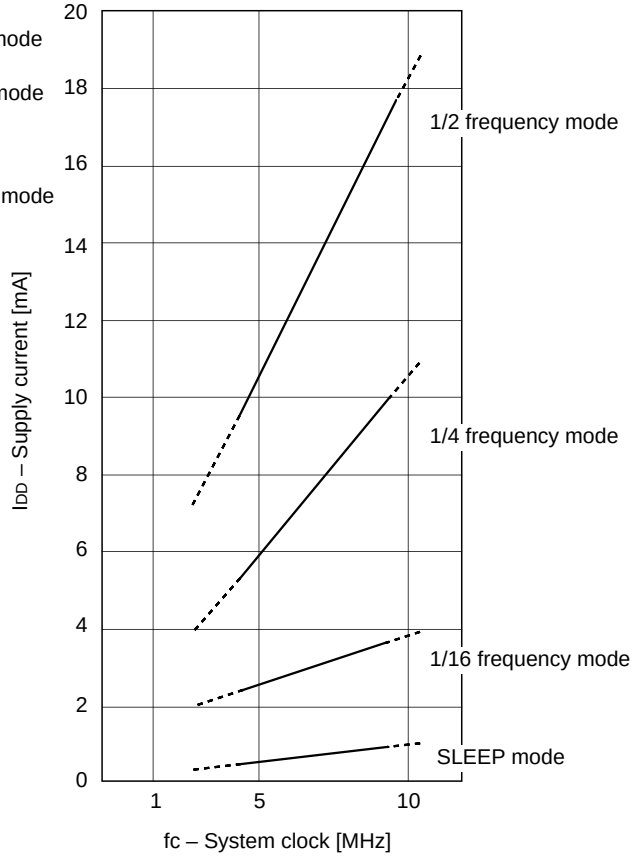
* The font data for the one-time PROM version is operated in the same way as the program writing.

Fig. 14. Characteristics curves

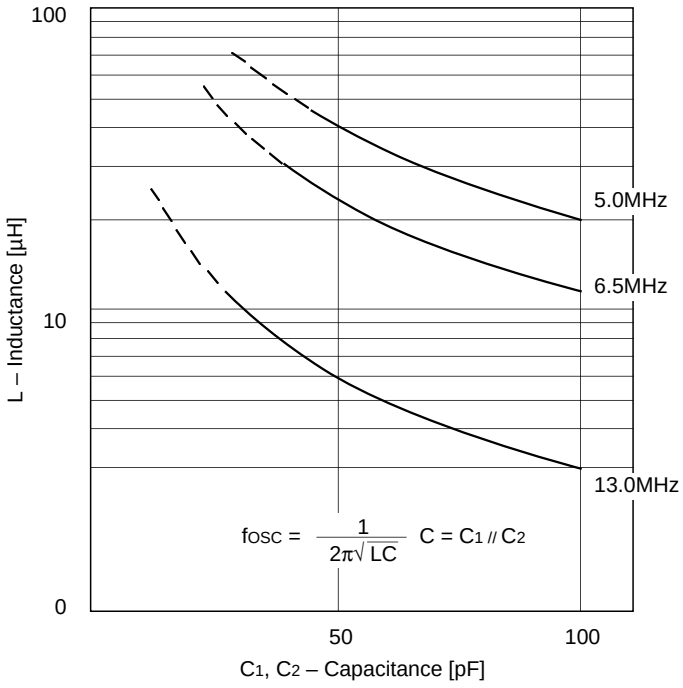
IDD vs. VDD
(fc = 8MHz, Ta = 25°C, Typical)



IDD vs. fc
(VDD = 5V, Ta = 25°C, Typical)



Parameter Curve for OSD Oscillator L vs. C
(Analytically calculated value)

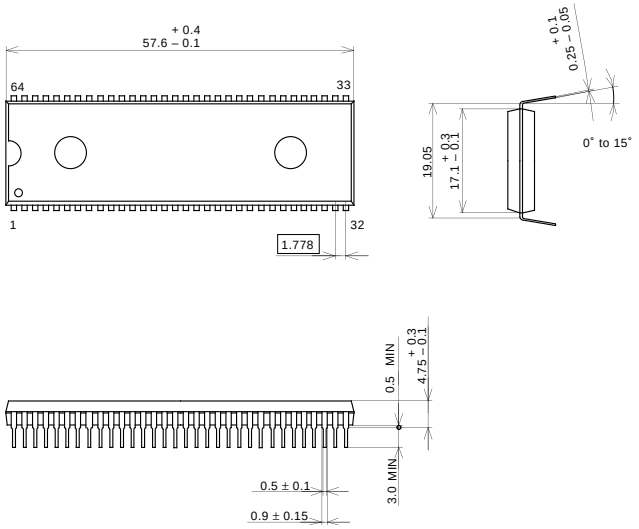


$$f_{OSC} = \frac{1}{2\pi\sqrt{LC}} \quad C = C_1 // C_2$$

Package Outline

Unit: mm

64PIN SDIP (PLASTIC)

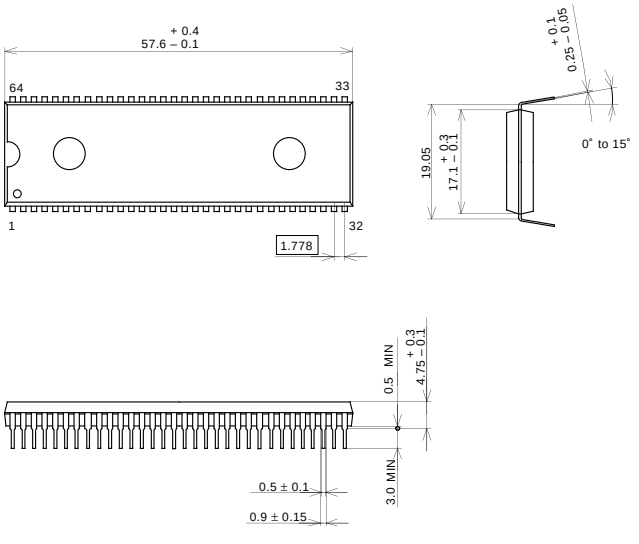


SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

64PIN SDIP (PLASTIC)



SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

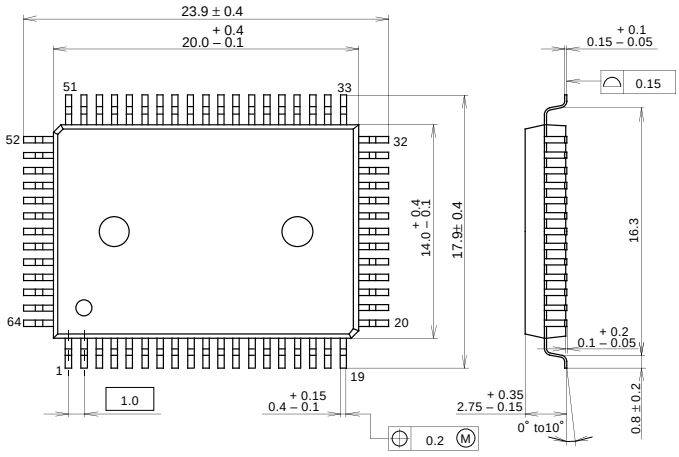
LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm

Package Outline

Unit: mm

64PIN QFP (PLASTIC)

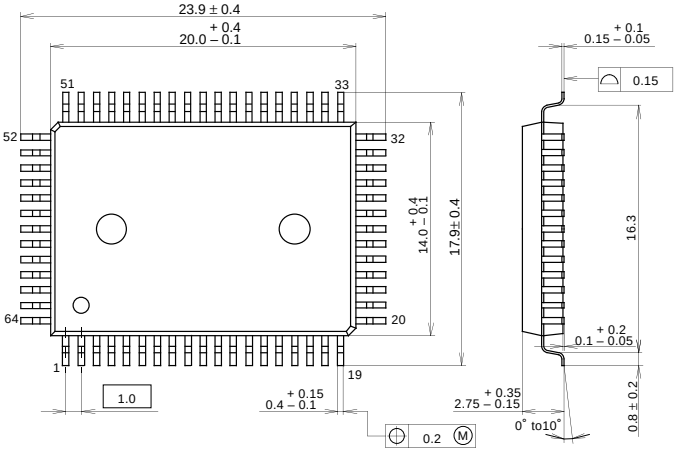


PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	P-QFP64-14x20-1.0
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

64PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	P-QFP64-14x20-1.0
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18μm